PATENT ABSTRACTS OF JAPAN

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(21)Application number : 62-111914
(22)Date of filing : 08.05.1987

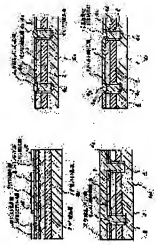
(71)Applicant : NEC CORP
(72)Inventor : TAKEMURA HISASHI

(54) SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

(57)Abstract:

PURPOSE: To enable an element to be constructed finely, by utilizing a polycrystalline silicon film used for filling a trench isolating groove also for a highly doped region located directly below an aperture for leading out a substrate potential.

CONSTITUTION: On a P-type silicon substrate 1, there are provided an N+type buried layer 2, an N-type epitaxial layer 3, a silicon oxide film 7', a silicon nitride film 8, a silicon oxide film 9 and a patterned resist film 10. Then, grooves are excavated vertically by the RIE process for providing trench isolating grooves 4. The structure is subjected to thermal oxidation and RIE so that a silicon oxide film 4a is left only on the side walls of the grooves. A polycrystalline silicon film 11 is then deposited all over the surface. The structure is subjected to etching back and thermal oxidation in order to provide polycrystalline silicon films 4b filling the grooves, a silicon oxide film 12 and a high-concentration P+ buried layer 4c. Finally, a field oxide film 7 and apertures 6 for leading out a substrate potential are provided.



PATENT ABSTRACTS OF JAPAN

(11)Publication number : 2000-269317
(43)Date of publication of application : 29.09.2000

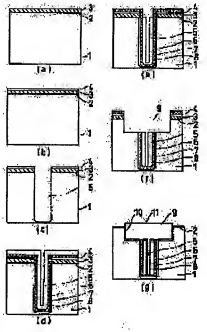
(51)Int.Cl. H01L 21/76

(21)Application number : 11-067372
(22)Date of filing : 12.03.1999

(71)Applicant : TOSHIBA CORP
(72)Inventor : TSUKIHARA TETSUYA

(54) SEMICONDUCTOR DEVICE AND ITS MANUFACTURE

(57)Abstract:
PROBLEM TO BE SOLVED: To reduce parasitic capacitance in a trench isolation structure by a method wherein isolation films of at least three layers or more are provided on a side wall of a trench.
SOLUTION: A deep trench side wall oxide film 6 of 50 nm and a side wall TEOS film 7 of 200 nm are formed in a side wall of a deep trench 5. Next, a shallow trench 9 is formed, and after a resist is removed, a semiconductor substrate 1 is etched. Here, a buried poly-silicon 8 in the bottom of the deep trench 5 is completely removed when the shallow trench 9 is etched, and the deep trench 5 is completely isolated. Next, in order to protect the side walls of the shallow trench 9 a shallow trench side wall oxide film 10 of 50 nm is formed. Simultaneously, a clearance of the buried poly-silicon 8 inside the deep trench 5 is also oxidized. Thereafter, a buried TBOS film 11 of the shallow trench 9 is formed by a LP-CVD method, to bury a clearance remained behind slightly in a burying part of the deep trench 5.



PATENT ABSTRACTS OF JAPAN

(11)Publication number : 2001-110890
(43)Date of publication of application : 20.04.2001

(51)Int.Cl. H01L 21/76

(21)Application number : 2000-283497
(22)Date of filing : 15.12.1989

(71)Applicant : SONY CORP
(72)Inventor : GOMI TAKAYUKI
NAKAMURA MINORU
KASHIWANUMA AKIO
MIWA HIROYUKI
ITABASHI MASAO

(54) SEMICONDUCTOR DEVICE AND ITS MANUFACTURING METHOD

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a semiconductor device and its manufacturing method which comprises a trench separation region that can suppress the stress to a semiconductor base body and an occurrence of crystal defect.
SOLUTION: A semiconductor device 1 comprises a trench separation region 3. In the trench separation region 3, a channel 4 formed at a semiconductor base body 1 is filled with a polycrystal semiconductor layer 6 to a specified depth through an insulating film 5 while an oxidation-resistance film 8 and an insulating layer 9 are formed on the polycrystalline semiconductor layer 6 to fill the channel 4.